In the Abstract:

Please amend the Abstract as follows:

~~This patent describes a~~ A boundary scan system ~~where~~ includes memories, i.e. flip flops or latches, used in shared data scan cells that are also used functionally, ~~but~~ and memories used in dedicated control scan cells that are dedicated for test and not used functionally. The control scan cells can be scanned while the circuit is in functional mode, since their memories are dedicated. However, the data scan cells can only be scanned after the circuit transitions into test mode, since their memories are shared. This boundary scan system advantageously provides; (1) lower test circuitry overhead since the data scan cells use shared memories, (2) safe entry into test mode since the control scan cells can be scanned during functional mode to pre-load safe control conditions, and (3) avoidance of floating (i.e. 3-state) busses that can cause high current situations. A multiplexer selectively connects the shared data scan cells in series with the dedicated control scan cells to provide a scan path through all the scan cells during test mode. Resynchronization memories can be used between the dedicated control scan cells and the multiplexer to eliminate hold and set-up time problems.